ABSTRACT

A frequency synthesizer that includes two fractional dividers, two noise-shaped quantizers, three integer dividers, a PLL, an algorithm embodied in control logic, and an adjustment means. The noise-shaped quantizers are used to quantize two fractional (fixed-point) values, derived from the divider control words, into time-varying values. The dividers and PLL are used to generate an output signal by means of multiplying a reference signal by the quotient of the divider control word values. Accordingly, the frequency synthesizer of the present invention can provide a very precise output clock, with the average output frequency being the input frequency multiplied by the quotient of the two divider control words, and with high jitter stability.